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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Herbert Palm et al.
CIP of
Applic. No. : 09/900,654, filed July 6, 2001
CIP filed : August 9, 2001
Title : Memory Cell, Memory Cell Configuration and Fabrication Method

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 5,768,192 (Eitan), dated June 16, 1998;

U.S. Patent No. 6,011,725 (Eitan), dated January 4, 2000;

U.S. Patent No. 6,191,459 B1 (Hofmann et al.), dated February 20, 2001;

German Published, Non-Prosecuted Patent Application No. DE 196 00 423 A1 (Hofmann et al.), dated July 17, 1997, electrically programmable memory cell configuration and method for its production;

German Published, Non-Prosecuted Patent Application No. DE 195 45 903 A1 (Krautschneider et al.), dated June 12, 1997, read-only memory cell configuration and method for its production;

German Patent No. DE 196 00 422 C1 (Krautschneider et al.), dated August 21, 1997, electrically programmable memory cell configuration and method for its production;

German Patent No. DE 196 03 810 C1 (Krautschneider et al.), dated August 28, 1997, memory cell configuration and method for its production;

International Publication No. WO 99/60631 (Eitan et al.), dated November 25, 1999;

"A Sub-0.1- μ m Grooved Gate MOSFET with High Immunity to Short-Channel Effects" (Tanaka et al.), IEDM 93, Chapter 21.1.1, pp. 537-40;

"A Flash EEPROM Cell with Self-Aligned Trench Transistor & Isolation Structure"
(Nakagawa et al.), 2000 Symposium on VLSI Technology Digest of Technical Papers.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,



For Applicants

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